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DESIGN AND IMPLEMENTATION OF A PLL USING CSVCO IN 180 nm CMOS TECHNOLOGY

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Abstract
In this work, a current-starved voltage controlled oscillator (CSVCO) has been implemented in an XOR-phase detector based phase locked loop (PLL) using 180 nm CMOS technology with a supply voltage of 1.8 V. The design has been analyzed and its performance has been validated by using appropriate simulations in Cadence. The power dissipated by the PLL is around 2.197 mW with a phase noise level of about -127.356 dBc/Hz at an operating frequency of 200 MHz. It consumes a die area of appropriately 3440.882775 μm^2. A physical layout of the design has been obtained.

Index Terms: Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO), Phase Detector, Loop Filter, Phase Difference, Phase Noise, Power Dissipation.

1. Introduction

A phase locked loop (PLL) is a feedback system that compares the output phase with the input phase. It is a control system that tracks the change in phase of feedback signal with respect to that of the reference signal once it is locked. This comparison of phase is performed by phase detector. A phase detector is a circuit whose average output varies monotonically with phase difference between its two inputs. The output of phase detector is filtered by the low pass filter which provides a dc level at the input of voltage controlled oscillator (VCO). This signal acts as the control voltage for the VCO which is responsible for frequency tuning in the PLL. This output frequency of the VCO varies accordingly to match with phase of the reference signal. Frequency tuning occurs till the PLL achieves lock state. Once it is locked it tries to track the phase difference between the reference and the feedback signals.

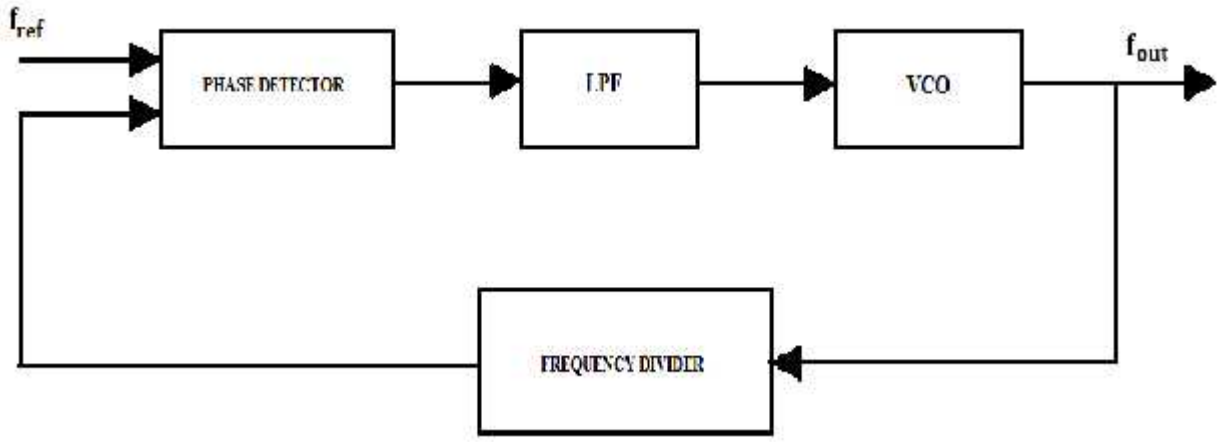

Fig.1. Block diagram of a phase locked loop (PLL)

A PLL contains three basic building blocks as shown in figure() such as,

1. Phase detector
2. Loop filter
3. VCO

The phase detector compares the phase of input signal or reference signal with the phase of signal produced by the VCO and generates an output signal proportional to the time difference between the two. The difference voltage signal is filtered by the loop filter and is applied to the input of the VCO. The control voltage on the VCO produces the frequency such that it reduces the phase difference between the input signal and the local oscillator.
Generally, a PLL undergoes through three states, such as,

- **Free-Running:** With no input signal applied to the PLL system, it is said to be in free-running state.
- **Capture:** the PLL is said to be in capture state when it compares the reference frequency with that of the feedback and tries to bring the loop to lock state.
- **Phase Lock:** The loop is said to be locked if the phase difference between reference and feedback signal does not change with time.

Major drawback of this type of PLL is that duty cycle of VCO output clock needs to be 50%. Although it has some limitations but one may be forced to use this type of PLL for some specific applications such as data and clock recovery. The advantage of using this type of PLL is that it provides a good noise rejection as output of the phase detector gets averaged or integrated by the low pass filter used.

The remaining sections of the paper are organized as follows. In the next section, the phase detector has been characterized and designed. This is followed by sections III and IV presenting the design and analysis of loop filter and VCO respectively. In section V, all these fundamental blocks have been implemented in a PLL and its output and performance have been validated through appropriate simulations carried out in Cadence. Finally, the performance of the PLL has been summarized and the findings have been concluded in the conclusion section.

2. Phase Detector

Phase detector is a circuit whose output is linearly proportional to phase difference between its two input signals. Here, an XOR-phase detector has been used as shown in figure 2. Its two inputs are the reference signal and the feedback signal. The reference signal generally comes from a quartz crystal oscillator, whereas, the feedback signal comes from the output of VCO or an optional divider used in the feedback path. XOR-phase detector is designed using a simple XOR-gate which takes reference and feedback as its two inputs and gives the phase difference between the two as its output. The width of the output pulse is proportional to the phase difference between the two input signals. The phase detector has been characterized for different phase differences by performing appropriate simulations in Cadence as shown in figure 3 to figure 6.

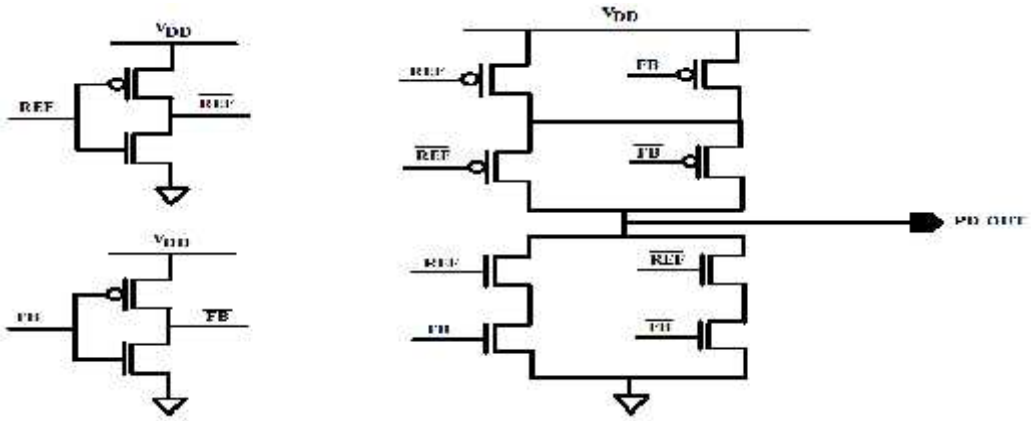

Fig.2. Schematic of XOR-phase detector

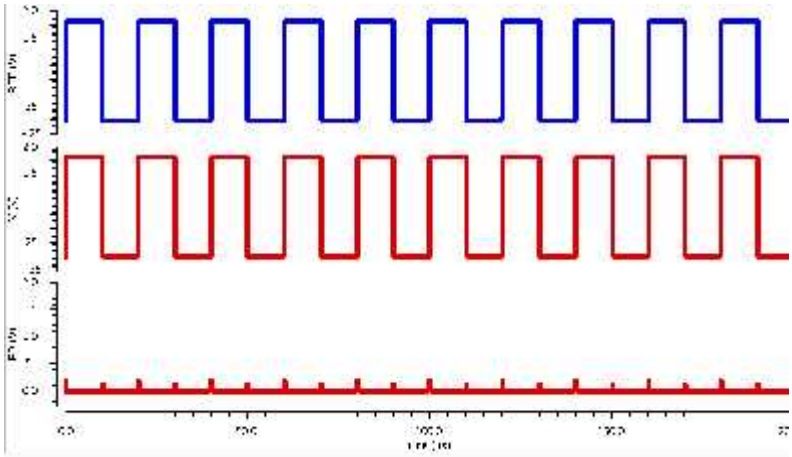

Fig.3. Output waveform of phase detector when Δϕ=0

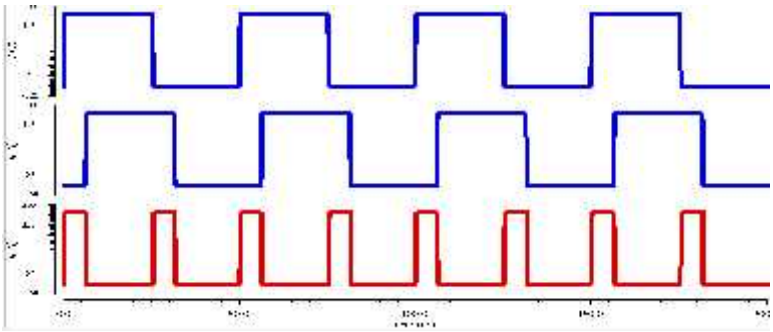

Fig.4. Output waveform of phase detector when Δϕ=3π/4

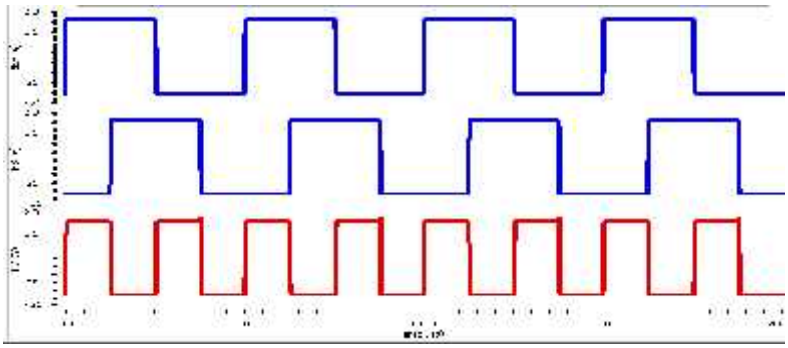

Fig.5. Output waveform obtained for phase detector when Δϕ=π/2

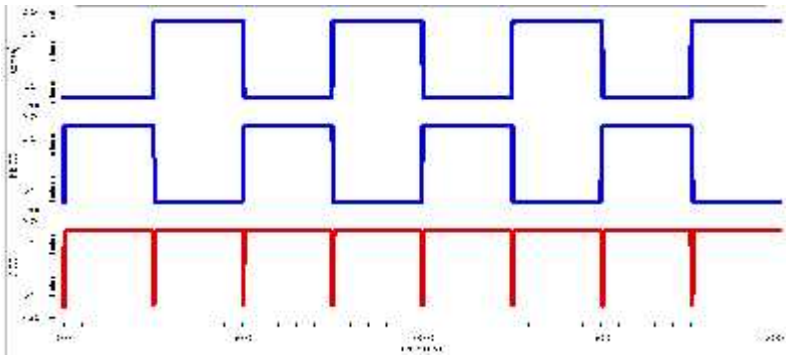

Fig.6. Output waveform obtained for phase detector when Δϕ=π

3. Loop Filter

Output of phase detector is averaged by the low pass filter. It provides a dc level at the VCO input. Generally, a first order low pass filter is being used in this work. The schematic of the low pass filter has been shown in figure 7.

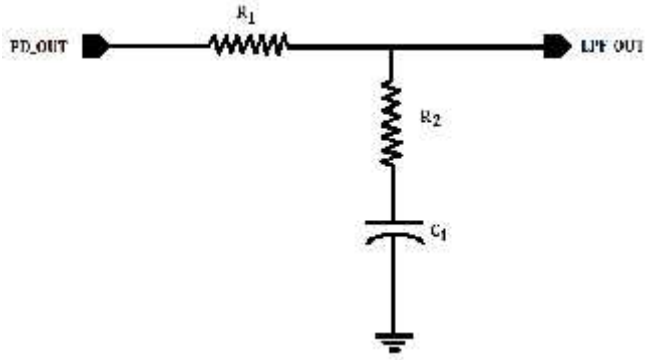

Fig.7. Schematic of low pass filter

4. Voltage Controlled Oscillator (VCO)

VCO is an electronic oscillator whose output frequency linearly varies with the input control voltage. The output of loop filter acts as the input control voltage and frequency is controlled accordingly. It is the heart of the PLL system. The noise performance and power dissipation of the PLL is determined by the VCO as it is the most power consuming element and acts as a main source of noise.

In this work, a five-stage CSVCO has been used for the design of PLL and its schematic has been represented as shown in figure 8. The graph representing variation of oscillation frequency with respect to change in control voltage has been depicted in figure 10 using the data depicted in table 1. It represents tuning range of the VCO.

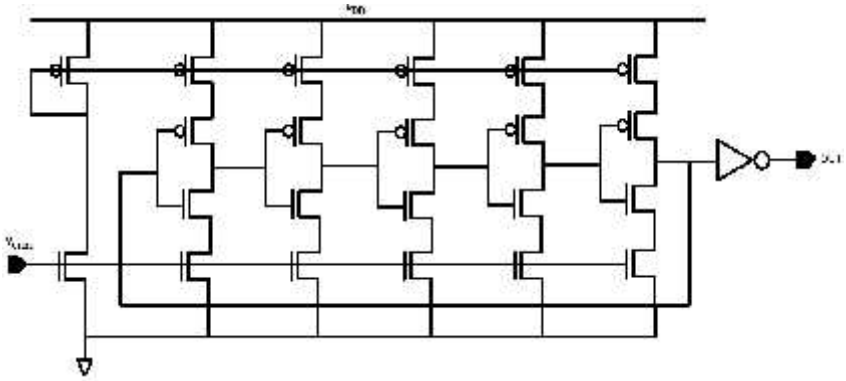

Fig.8. Schematic of current-starved VCO

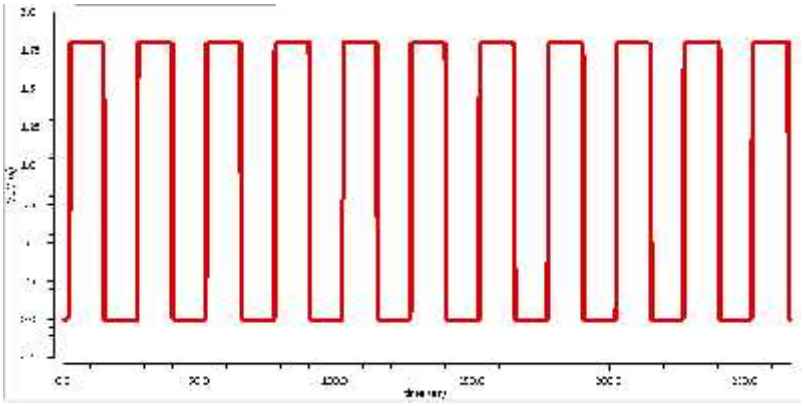

Fig.9. Output waveform obtained for the VCO at 200 MHz operating frequency

Table 1: Tuning range

V_{inVCO} (volts)	Frequency(MHz)
0.5	20.4
0.6	108.0
0.7	315.1
0.8	577.5
0.9	822.6
1.0	1027
1.1	1185
1.2	1303
1.3	1388
1.4	1450
1.5	1490
1.6	1527
1.7	1552
1.8	1572

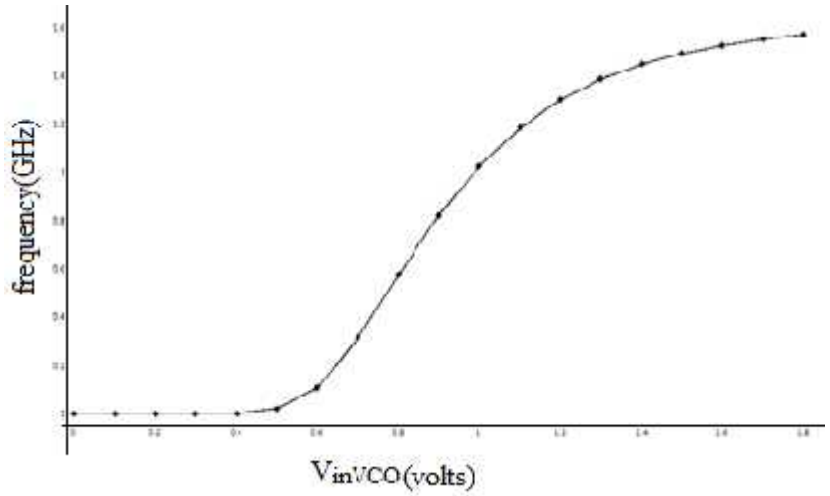

Fig.10. Variation of oscillation frequency with respect to input control voltage

5. PLL Design and Performance Analysis

All the above blocks are integrated to form the PLL structure. A system level simulation is performed in Cadence.
The design parameters to be considered are as follows,

- Delay
- Power dissipation
- Phase noise
- **Lock Range:** The range of frequencies over which the PLL can maintain this locked condition is defined as the ***lock range*** of the system.

Lock range is given as-

$$\Delta\omega_L = \pi\zeta\omega_n \quad (1)$$

where
ζ = damping factor
ω_n= natural frequency

- **Capture Range:** The lock range always is larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the ***capture range*** of the PLL system.

Lock time: Lock time is given by,

$$T_L = \frac{2\pi}{\omega_n} \quad (2)$$

The output waveforms of PLL has been depicted in figure 14.

The phase noise was obtained to be -127.356 dBc/Hz at 1 MHz offset frequency from the carrier as seen in figure 16. Layout of the PLL has been obtained and is shown in figure 17.

For subsequent analysis of PLL, the phase-lock condition must be defined carefully. The loop is said to be locked if " $\Phi_{out} - \Phi_{in}$" does not change with time which can be expressed mathematically as:

$$\frac{d\Phi out}{dx} - \frac{d\Phi in}{dx} = 0 \quad (3)$$

and hence,

$$\omega_{out} = \omega_{in} \quad (4)$$

where
Φ_{out} = phase of output clock; Φ_{in} = phase of reference clock
ω_{out} = frequency of output clock; ω_{in} = frequency of reference clock

Two quantities are considered to be unknown: Static phase error "Φ_0" and dc level of "V_{cont}".

These values could be determined from the phase detector and VCO characteristics.

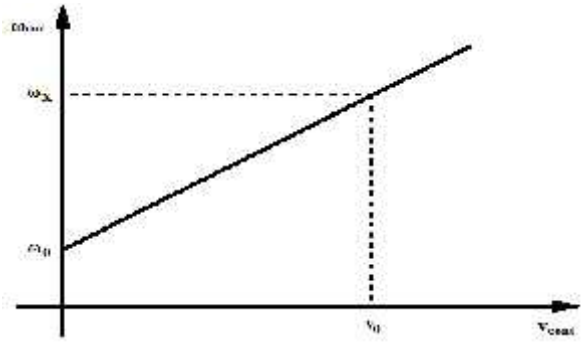

Fig.11. VCO characteristic plot

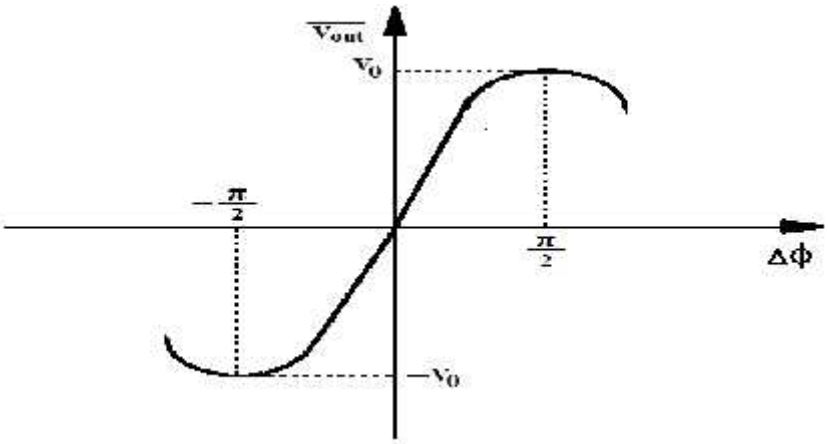

Fig.12. Characteristic plot of phase detector

Since $$\omega_{out} = \omega_0 + K_{VCO}\, V_{cont} \quad (5)$$

and $$V_{PD\_out} = \overline{K_{PD}}\, \Delta\Phi \quad (6)$$

we have,

$$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}} \quad (7)$$

and $$\Phi_0 = \frac{V_1}{K_{PD}} = \frac{\omega_1 - \omega_0}{K_{PD} K_{VCO}} \quad (8)$$

Considering a PLL in locked condition and assuming the input and output waveforms that can be expressed as:

$$V_{in}(t) = V_A \cos \omega_1 t \quad (9)$$

$$V_{out}(t) = V_B \cos(\omega_1 t + \Phi_0) \quad (10)$$

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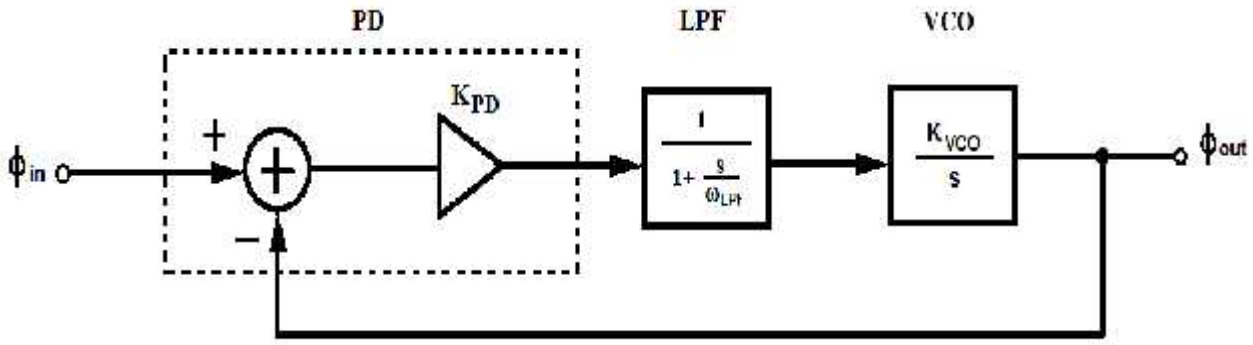

Fig.13. linear model of type-1 PLL

Transfer function of low pass filter (LPF) is given by,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+\frac{s}{\omega_0}} \quad \textbf{(11)}$$

Phase detector output contains a dc component which is given by,

$$\mathbf{V_{PD\_out} = K_{PD}\,(\Phi_{out} - \Phi_{in})} \quad \textbf{(12)}$$

and high frequency components.

$$\text{LPF Transfer function} = \frac{1}{1+\frac{s}{\omega_{LPF}}} \quad \textbf{(13)}$$

where

ω_{LPF} ➔ -3dB Bandwidth

$$\text{VCO Transfer function} = \frac{K_{VCO}}{s} \quad \textbf{(14)}$$

If
Φ_{in} ➔ Excess phase of input waveform
Φ_{out} ➔ Excess phase of output waveform

then
Open loop transfer function of PLL is given by,

$$\mathbf{H(s)|_{open}} = \frac{\Phi out}{\Phi in}\mathbf{(s)|_{open}}$$

$$= \mathbf{K_{PD}} \frac{1}{1+\frac{s}{\omega_{LPF}}} \frac{K_{VCO}}{s} \quad \textbf{(15)}$$

revealing one pole at s = − ω_{LPF} and another at s=0.
s = − ω_{LPF}
and s = 0

⇨ **Loop gain = $H(s)|_{open}$**

Since loop gain contains a pole at origin, the system is called “type-I”.

From above equation we can write the closed-loop transfer function as-

$$\mathbf{H(s)|_{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}} \quad \textbf{(16)}$$

$$\Rightarrow \frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

Therefore, it is seen that if ω_{in} changes very slowly ($s \rightarrow 0$), then ω_{out} tracks ω_{in} if loop is assumed to be locked. Since change in ω_{out} must be accompanied by a change in V_{cont}, we have,

$$H(s) = K_{VCO}\frac{V_{cont}}{\omega_{in}}(s) \quad (17)$$

The above expression for closed loop transfer function can be expressed by,

$$\mathbf{H(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (18)$$

where

$$\boldsymbol{\omega_n} = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \quad (19)$$

$$\boldsymbol{\zeta} = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \quad (20)$$

The two poles of the closed loop system are given by,

$$\mathbf{s_{1,2}} = -\boldsymbol{\zeta}\,\boldsymbol{\omega_n} \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$$

$$= (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n \quad (21)$$

If $\zeta > 1$ ➔ both poles are real, the system is over-damped
If $\zeta < 1$ ➔ poles are complex and response to an input frequency step $\omega_{in} = \Delta\omega\, u(t)$ is equal to

$$\boldsymbol{\omega_{out}(t)} = \{1 - e^{-\zeta\omega_n t}[\cos(\omega_n\sqrt{1-\zeta^2}\,t) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}\,t)]\}\Delta\omega\, u(t)$$

$$= [1 - \frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin(\omega_n\sqrt{1-\zeta^2}\,t + \Theta)]\Delta\omega\, u(t) \quad (22)$$

where
ω_{out} ➔ change in output frequency
Θ➔ $\sin^{-1}\sqrt{1-\zeta^2}$

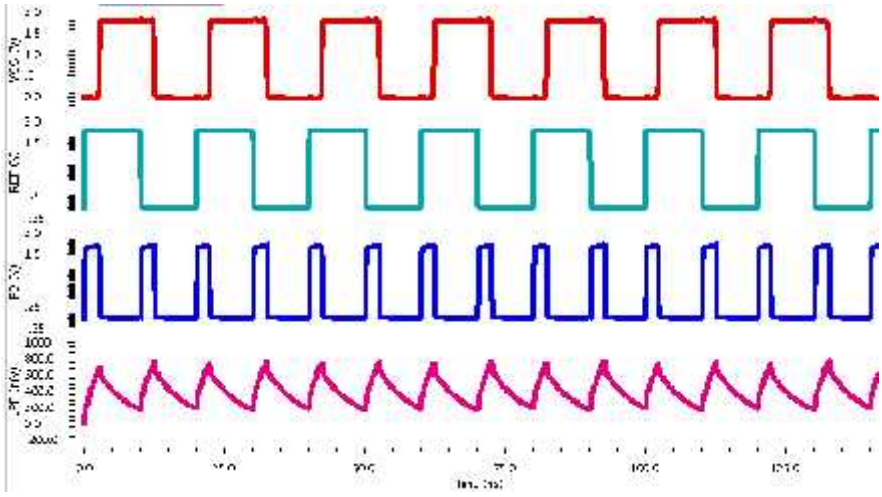

Fig.14. Output waveform of PLL during lock state

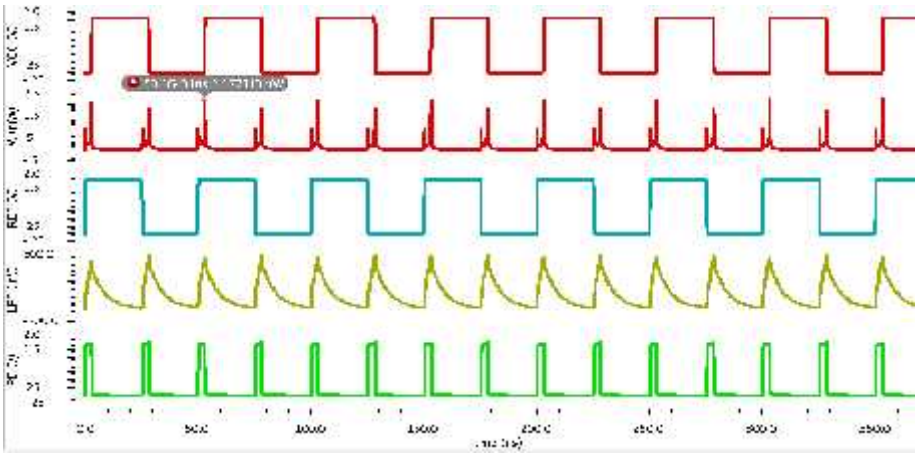

Fig.15. Power estimation in Cadence for PLL in lock state

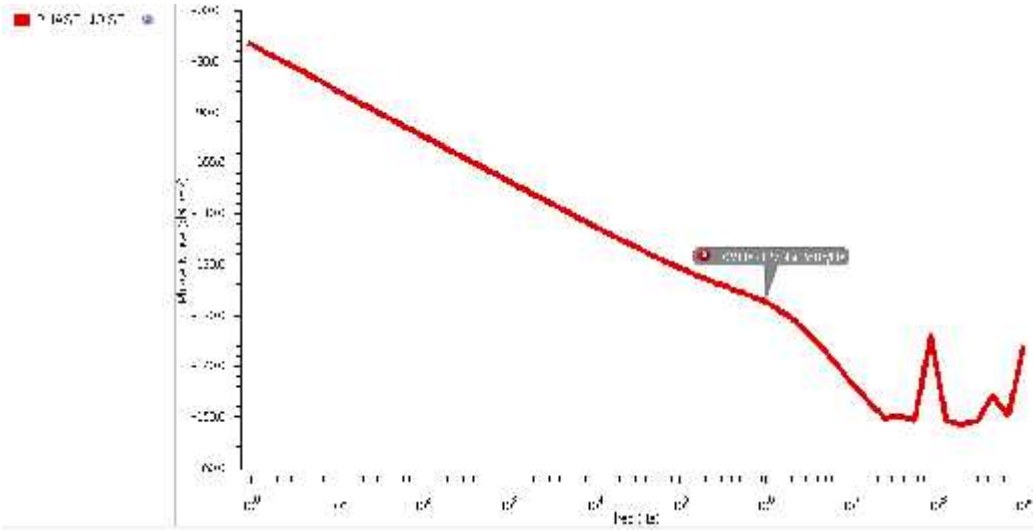

Fig.16. Phase noise obtained at 1 MHz offset frequency from the carrier

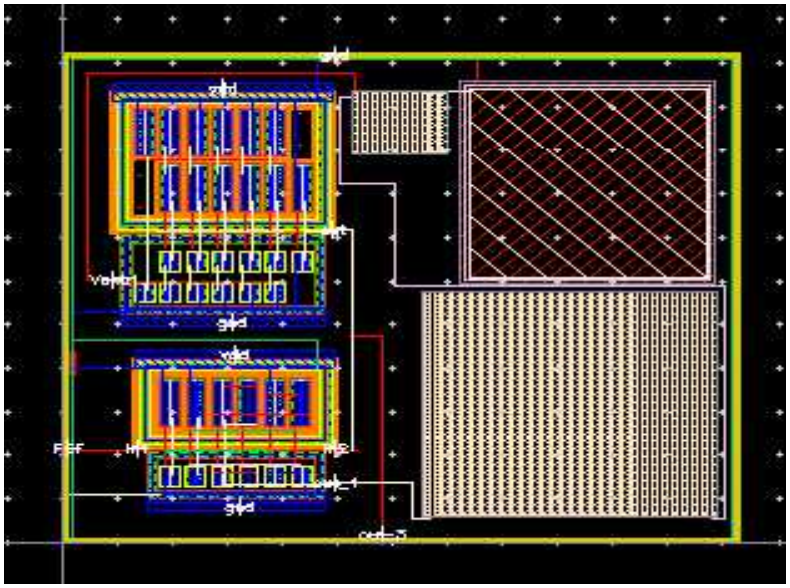

Fig.17. Layout of PLL

Table 2: Performance summary and comparison

Parameters	Ref[8]	Ref[9]	This work
Technology (CMOS)	180 nm	250 nm	180 nm
Operating voltage (V)	1.8	2.5	1.8
Operating frequency (MHz)	-	-	200 MHz
Type	II	-	I
Order	1	-	1
Lock range	50 MHz – 1GHz	-	20 MHz – 600 MHz
Settling time (ns)	265	1500	<50
Phase noise (dBc/Hz)	-	-	-127.356
Power dissipation (mW)	0.2772	3.875	2.197
VCO gain (GHz/V)	2.21	-	2.373
Die area (μm^2)	-	45666.5	3440.882775

6. Conclusion and Future Scope

The design has been presented in a 180nm CMOS technology and is designed using a current-starved voltage controlled oscillator (CSVCO). The PLL dissipates power of around 2.197 mW for 1.8 V supply with a phase noise of -127.356 dBc/Hz. The overall area consumed is about 3440.882775 μm^2. This work can be extended further by optimizing the design to achieve improved performance for different applications. The VCO can also be implemented in a charge-pump PLL. In addition, the design could be implemented for low power applications in the future.

7. References

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