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DESIGN AND ANALYSIS OF AN ULTRA-LOW POWER VCO USING 180 nm CMOS TECHNOLOGY

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Abstract
In this paper, a five-stage current-starved voltage-controlled oscillator (CSVCO) has been designed for ultra-low power, low frequency applications. A tuning range of 79.95% is achieved with a phase noise level of -92.25 dBc/Hz at 1 MHz offset frequency from the carrier. The power dissipation has been reduced up to 939.5546 NW at 32.41 MHz frequency of oscillation. The performance of the circuit has been analyzed and is validated by carrying out simulations for transient and noise analysis in Cadence tools using 180 nm CMOS process at a supply voltage of 0.6 V. Physical layout of the circuit has been obtained.

Index Terms: CMOS ring oscillator, current-starved VCO, tuning range, sub threshold regime, near-threshold region, power dissipation, control voltage, Phase locked loop.

I. Introduction

VCO is an electronic oscillator where oscillation frequency is controlled by an input voltage. An ideal VCO is a circuit whose output frequency is a linear function of its control voltage. VCOs are used for high speed clock generation, channel selection, frequency modulation and demodulation in various communication circuits. It is one of the important basic building blocks in analogue and digital circuits and is built as a part of high density IC (integrated circuit) system like transceiver and phase locked loops (PLLs) [1] [2] [3] as shown in figure 1. Ring VCO has wide range of frequency swing and easy to implement. In addition, it occupies less chip area as they do not have inductor as compared to LC-VCO. The important requirements of VCO are frequency accuracy, wide tuning range, tuning linearity, low power consumption, small size and low phase noise.

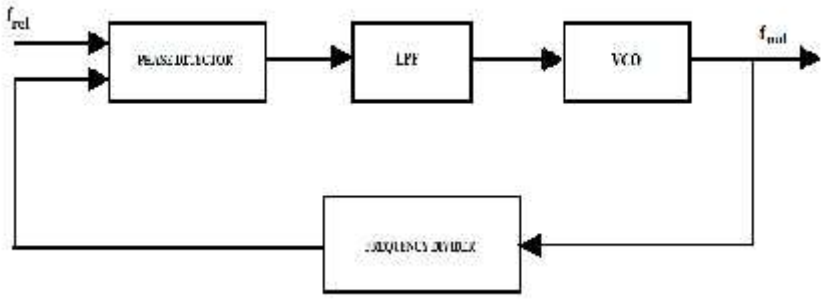

Fig.1: Block diagram of Phase Locked Loop

Wireless and wire-line communication systems such as wireless local area network, mobile and satellite communication, backplane interconnects and chip-to-chip communication systems, clock generation and skew compensation in microprocessors and other communication devices widely use PLL as a basic building block. The VCO jitter performance in these applications can impact the output clock's timing jitter which often limits the system performance. Also in most of the narrow band communication systems like frequency synthesizer plays a major role in generating local oscillation signal or carriers and is usually implemented through a PLL. The high power consumption in the frequency synthesizer is mainly due to the VCO. Therefore one of the most challenging building block of PLL is the VCO.

Optimization methodologies find wide scope for performance improvement in ICs design industry. The evolutionary optimization techniques have been widely applied for analogue ICs design. In modern VCOs, power consumption and frequency tuning are the key performance metrics [4][5]. Growing demand of portable devices like cellular phones, notebooks, personal communication devices have aggressively enhanced attention for the low power consumption. Power consumption in VLSI circuits includes dynamic, static power and leakage power consumption.

In VLSI, low power design problems can be broadly classified into two: analysis and optimization [6]. Analysis techniques serve as the foundation for design optimization. Analysis problems are concerned about the accurate estimation of the power or energy dissipation at different phases of the design process. Optimization is the process of generating the best design, given an optimization goal, without violating design specifications. Major criteria to be considered are the impact to the

circuit delay, which affects the performance and throughput of the chip and the chip area, which directly translates to manufacturing costs.

In nanotechnology, power has become the most important issue because of

(i) Increasing transistor count
(ii) Higher speed of operation
(iii) Greater device leakage currents.

As sub threshold conduction varies exponentially with gate voltage as shown in figure 2, it becomes more and more significant as MOSFETs shrink in size.

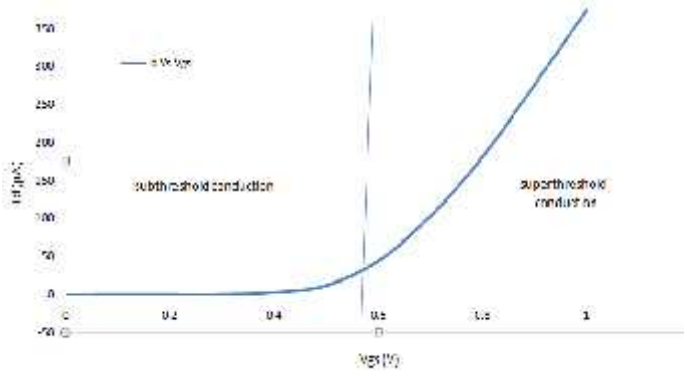

Fig.2: I_d versus V_{gs} curve showing subthreshold and superthreshold regions of operation.

There are several advantages of subthreshold region of operation, which can be listed as follows:

(i) Possibilities of achieving higher gain
(ii) Guaranteed low power consumption
(iii) Reduced distortion and improvement in linearity than saturation region
(iv) Increased output resistance

However, the major difficulty with subthreshold region of operation is the reduction in the circuit bandwidth and resulting frequency of operation. Energy-constrained applications such as wireless sensor nodes, RFID tags, medical equipments such as hearing aids and pace-maker, wearable computing or implants, personal digital assistants, energy scavenging applications, and laptops, which are dominated primarily by the need to minimize energy consumption and increase battery life time, speed is a secondary consideration for this class of applications, so subthreshold circuits offer a good solution.

However, it is worth mentioning that by optimizing the device structure to reduce intrinsic gate capacitances (C_{GS} and C_{GD}) frequency of operation can be increased. To meet low power specification without degrading the overall performance of the circuit near threshold region of operation is preferred over subthreshold regime. In this paper, the CSVCO has been designed to operate in near threshold region at a supply of 0.6 V using 180 nm CMOS technology. The remaining part of the paper has been organised as follows. The next section describes about the design objectives for the CSVCO. Section III elaborates the architecture and operation of the circuit. In section IV, the performance analysis of the circuit has been presented. Finally, the finding of the work has been concluded in section V.

II. Design Objectives For Csvco

The CSVCO is shown schematically in figure 6. The circuit has two distinct parts, the inverter stages (figure 3) and current-starving circuitry. The design objective of this work is to achieve low power without degrading the overall performance altogether subject to the physical constraints.

(i) Oscillation frequency

An N-stage CSVCO circuit in general produces oscillations at a frequency given by-

$$f_{osc} = \frac{I_d}{NC_{tot}V_{DD}} \quad (1)$$

where

N = Number of stages

$I_d = I_{d3} = I_{d4}$ = Center drain current

$$C_{tot} = C_{out} + C_{in} \quad (2)$$

$$C_{out} = C_{ox}'(W_pL_p + W_nL_n) \quad (3)$$

$$C_{in} = \frac{3}{2} C_{ox}'(W_pL_p + W_nL_n) \quad (4)$$

$$C_{tot} = \frac{5}{2} C_{ox}'(W_pL_p + W_nL_n) \quad (5)$$

VCO's output frequency (f_{clock}) is given by-

$$\omega_{clock} = 2\pi f_{clock} = K_{VCO} V_{ctrl} + \omega_0 \text{ (rad/sec)} \quad (6)$$

where
K_{VCO} = Gain or sensitivity of the circuit
V_{ctrl} = Input control voltage of the circuit
ω_0 = Intercept corresponding to $V_{ctrl} = 0$

(ii) Tuning range

VCO is designed such that its oscillation frequency is controlled by input voltage. Among other structures of VCO, ring oscillator has a large tuning range. Tuning range can be defined as-

$$\text{Tuning range \%} = \frac{f_{max} - f_{min}}{f_{center}} \times 100 \quad (7)$$

where
$f_{center} = f_{osc}$ = frequency of oscillation
f_{max} = maximum frequency
f_{min} = minimum frequency

(iii) Gain

Gain of the VCO is the slope of the curves given in figure 13. It is defined as-

$$K_{VCO} = 2\pi \left(\frac{f_{max} - f_{min}}{V_{max} - V_{min}}\right) \text{ rad/V-s} \quad (8)$$

where
V_{max} = maximum input voltage
V_{min} = minimum input voltage

(iv) Jitter

It is the interval between two times of maximum effect (or minimum effect) of a signal property that varies regularly with time. It is defined as-

$$\Delta t_{jitter} = \frac{1}{f_{center}} - \frac{1}{f_{center} + \Delta f_{VCO}} \quad (9)$$

where
Δf_{VCO} = Variation in the VCO's output frequency
f_{center} = frequency of oscillation

(v) Power dissipation

The total power dissipated by N-stage CSVCO circuit is given by-

$$P = P_{avg} + P_{sc} \quad (10)$$

where
P_{avg} = Average power dissipated by CSVCO which is given by-
$P_{avg} = V_{DD} I_{avg} = V_{DD} I_D$
P_{sc} = short circuit power dissipation

(vi) Phase Noise

The phase noise of the CSVCO circuit is expressed as-

$$L\{\Delta f\} = \frac{8}{3\eta} \frac{KT}{P} \frac{V_{DD}}{V_{char}} \frac{f_{osc}^2}{\Delta f^2} \quad (11)$$

Where

$V_{char} = \frac{\Delta V}{\gamma}$

P = Total power dissipated by the CSVCO (12
ΔV = Gate overdrive voltage

K = Boltzmann constant
T = Absolute temperature
γ = A coefficient which is 2/3 for long channel devices in saturation
η = Characteristic constant which is taken here as 1
Δf = Offset frequency from the carrier at which the phase noise is measured

(vii) Device sizing

In conventional logical effort calculations, the optimal ratio of PMOS width (Wp) to NMOS width (Wn) for achieving equivalent current drivability is approximately 2.5 : 1 due to the mobility deference between the carriers between the PMOS and NMOS devices. In addition, the effective width of a transistor in a stack of n devices is roughly 1/n in the strong-inversion region. Selection of the proper Wp:Wn ratio and effective width of stacked transistors is crucial for achieving optimal performance. It was found that the conventional logical effort framework based on strong-inversion operation fails to do so for subthreshold logic due to the difference in the transistor current behaviour. In the strong-inversion regime, drive current is a first-or second-order function of the four MOS terminal voltages. Whereas, the drive-current in subthreshold designs is an exponential function of the terminal voltages. Hence we need a new design paradigm for optimal device sizing based on the exponential current equation in the subthreshold region. The optimal PMOS to NMOS width ratio in the subthreshold regime decreases as compared to that of strong- inversion regime.

III. Circuit Description and Operation

The CSVCO is designed using ring oscillator and its operation is similar to it. A ring oscillator is comprised of a number of delay stages, with output of the last stage feedback to the input of the first as in figure 4. Delay cell can be designed with differential pair and CMOS inverter. In this paper, CMOS inverter is used as a delay cell as shown in figure 3. For oscillation to take place the ring oscillator must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage should provide phase shift of π/N, where 'N' is the number of delay stages. The remaining π phase shift is provided by dc inversion. Single ended oscillator requires odd number of stages for dc inversion. A single ended inverter based ring VCO block diagram is shown in figure 4.

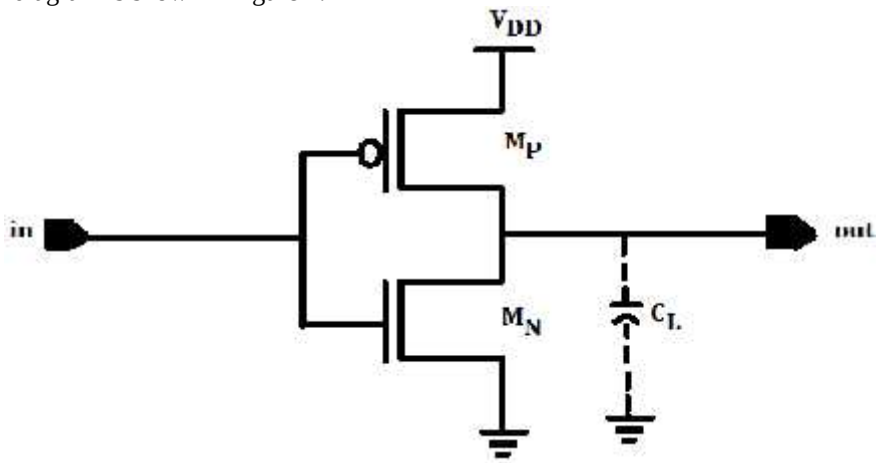

Fig.3: Inverter used (delay cell of ring oscillator)

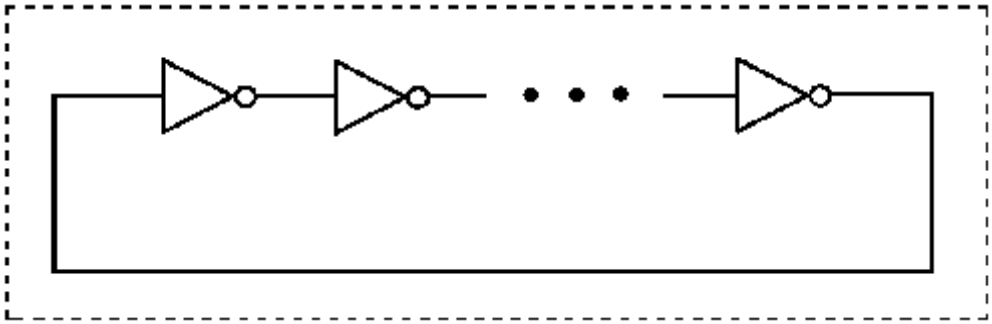

Fig.4: Block diagram Ring Oscillator

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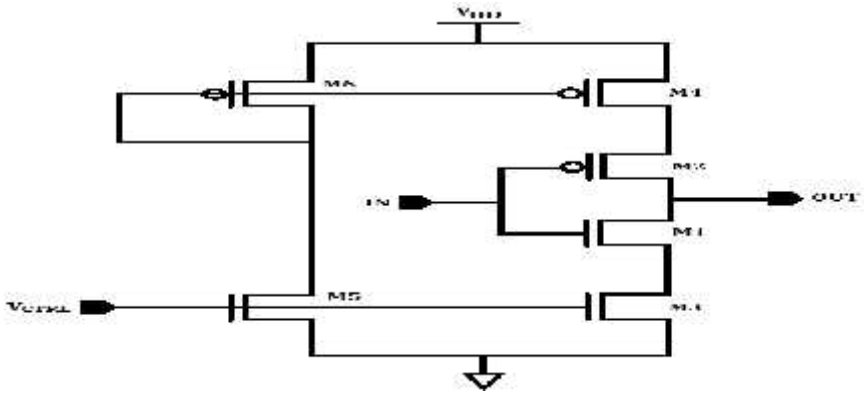

Fig.5: VCO delay cell

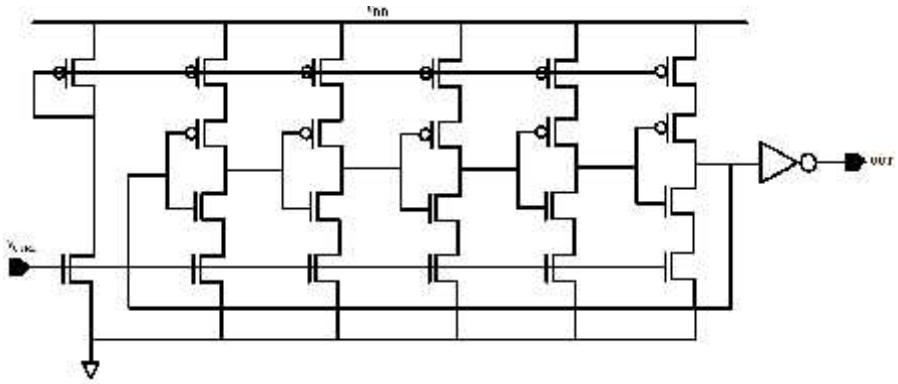

Fig.6: Schematic of 5-stage Current-Starved VCO

The operation of the CSVCO is same as the ring oscillator. MOSFETs M1 and M2 operate as an inverter, while MOSFETs M3 and M4 operate as current sources. The current sources, M3 and M4, limit the current available to the inverters, M1 and M2; in other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each current source stage. The output of the CSVCO is buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency.

IV. Performance Analysis

The inverter (delay cell) used in the design has been modelled and its corresponding VTC (Voltage Transfer Characteristic) has been obtained as shown in figure 7. The inverter has been simulated in Cadence and the corresponding simulation result has been depicted in figure 8. Its delay is found to be around 190.4 ps.

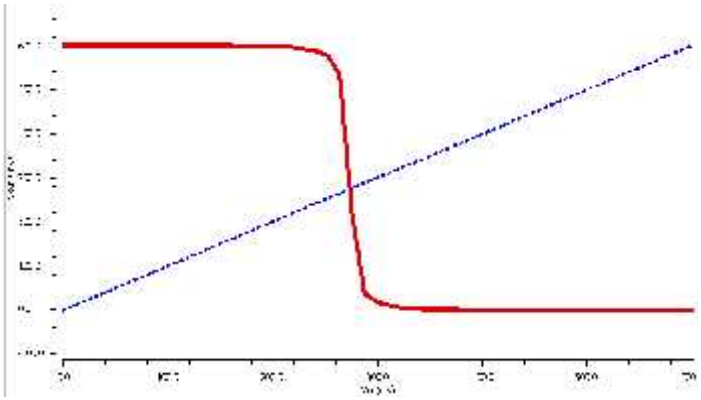

Fig.7: VTC of the inverter in subthreshold region obtained through DC analysis at a supply of 0.6 V

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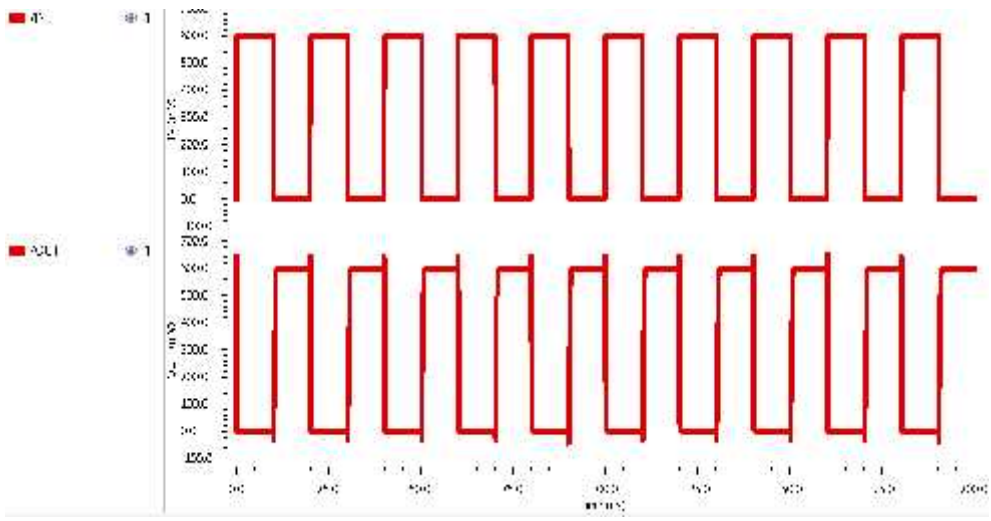

Fig.8: Verification of the inverter through simulation in Cadence using transient analysis

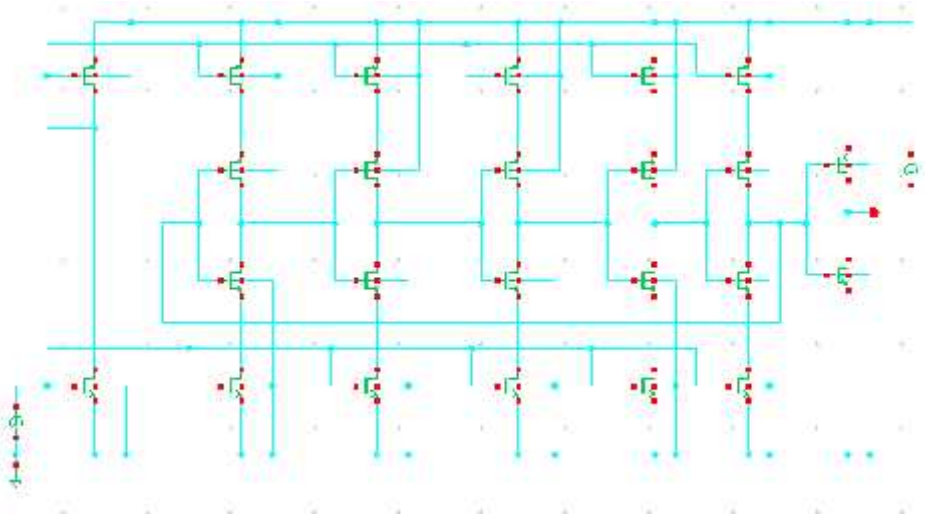

Fig.9: Implementation of Current-starved VCO in Cadence

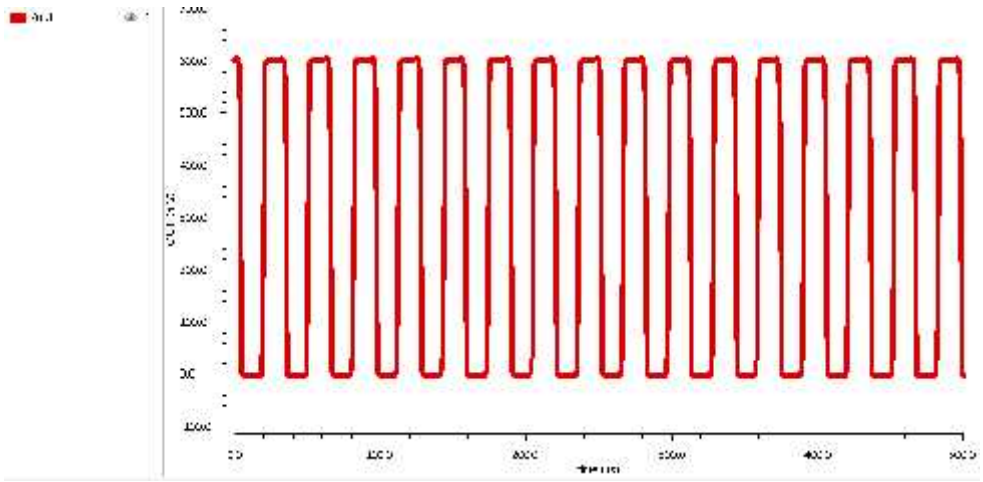

Fig.10: Output waveform of the VCO at an oscillation frequency of 32.41 MHz

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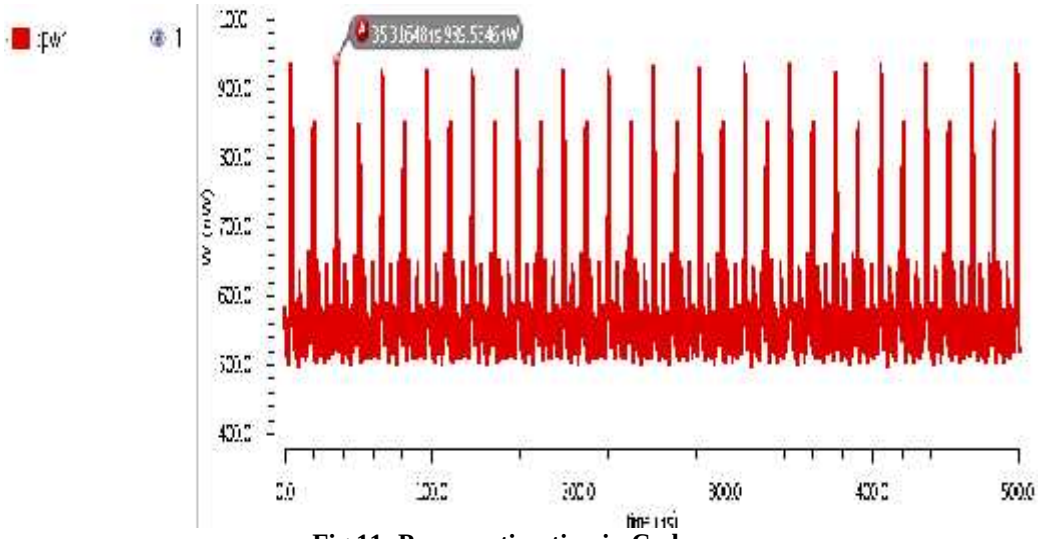

Fig.11: Power estimation in Cadence

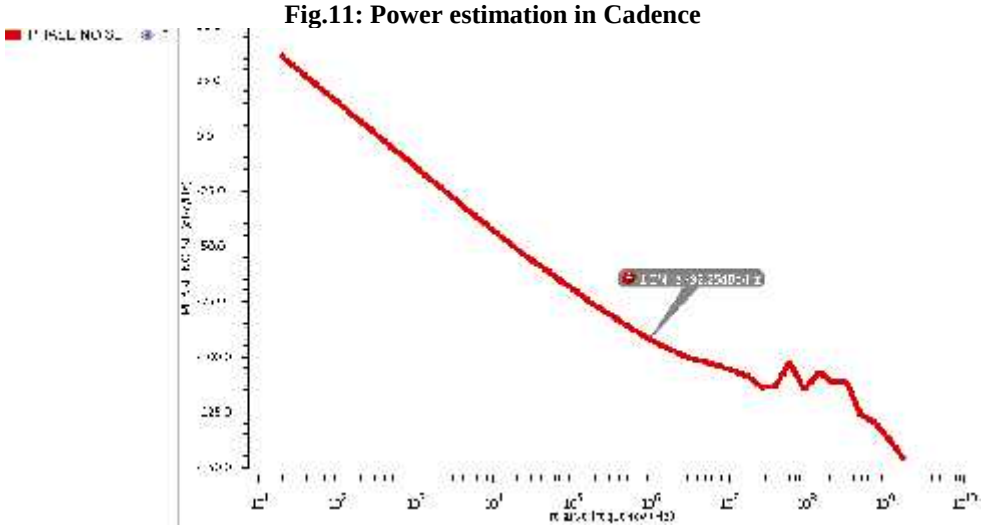

Fig.12: Phase Noise of around -92.25 dBc/Hz obtained for the current-starved VCO at 1 MHz offset frequency from the carrier

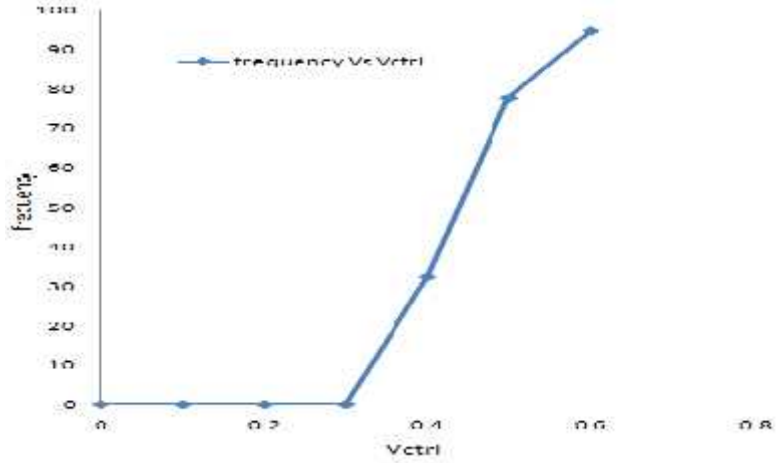

Fig.13: Graph showing variation of oscillation frequency with respect to control voltage

Table1. Tuning Range

V_{CTRL} (volts)	Frequency (MHz)	Power Dissipation (µW)
0.32	9.371	0.254
0.34	13.25	0.357
0.36	18.26	0.500
0.38	24.63	0.688
0.40	32.41	0.939
0.42	41.52	1.239
0.44	51.55	1.595
0.46	61.63	1.956
0.48	70.57	2.275
0.50	77.71	2.543
0.52	83.16	2.808
0.54	87.28	2.996
0.56	90.44	3.145
0.58	92.85	3.255
0.60	94.73	3.352

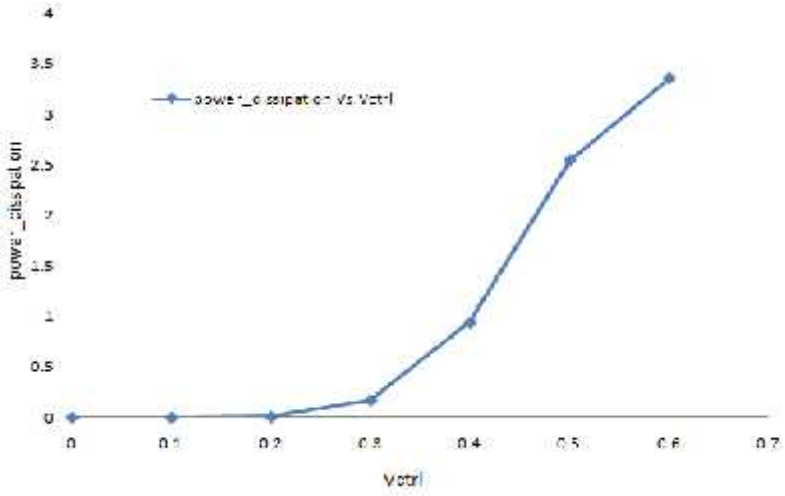

Fig.14: Plot showing variation of power dissipation with respect to control voltage

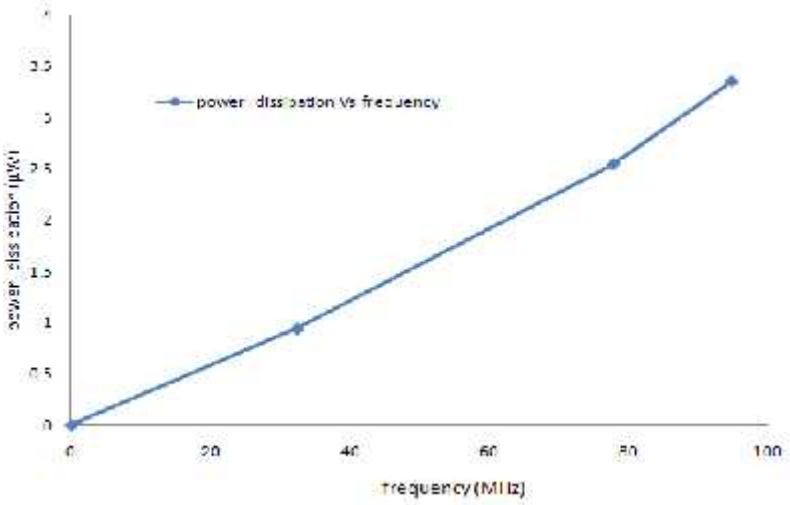

Fig.15: Power dissipation versus oscillation frequency plot

The CSVCO as shown in figure 9 has been simulated in Cadence Virtuoso Analog Design Environment using 180 nm CMOS technology to analyze performance of the circuit. The simulation of the physical design yields the oscillations depicted in figure 10 at a supply of 0.6 V having center frequency of about 56 MHz. Figure 12 shows phase noise plot which is obtained to be -92.25 dBc/Hz at 1 MHz offset frequency away from the carrier after performing appropriate noise analysis.
The oscillation frequency variation with control voltage is shown in figure 13 and the corresponding data is being provided in table 1. It could be seen that by varying control voltage from 0.32 V to 0.6 V the oscillation frequency range obtained is from 9.371 MHz to and 94.73 MHz and power dissipation varies from 0.254 µW to 3.352 µW with change in control voltage as well as frequency.

The power measurement for the CSVCO at an oscillation frequency of 32.41 MHz has been performed in Cadence environment and has been shown in figure 11.
The physical layout of the five-stage CSVCO is depicted in figure13.
Table 2 summarizes and compares the performance of the parameters with other approaches on the same circuit reported in [15]-[17].

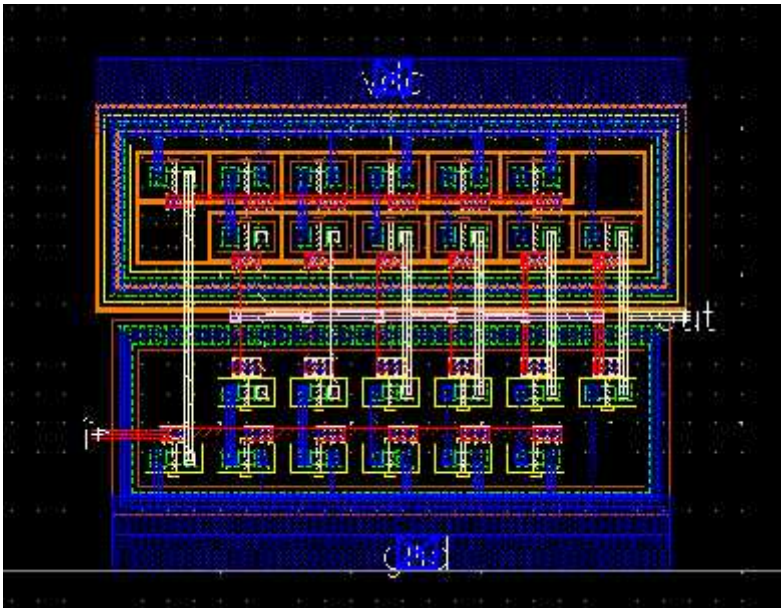

Fig.16: Layout obtained for the VCO

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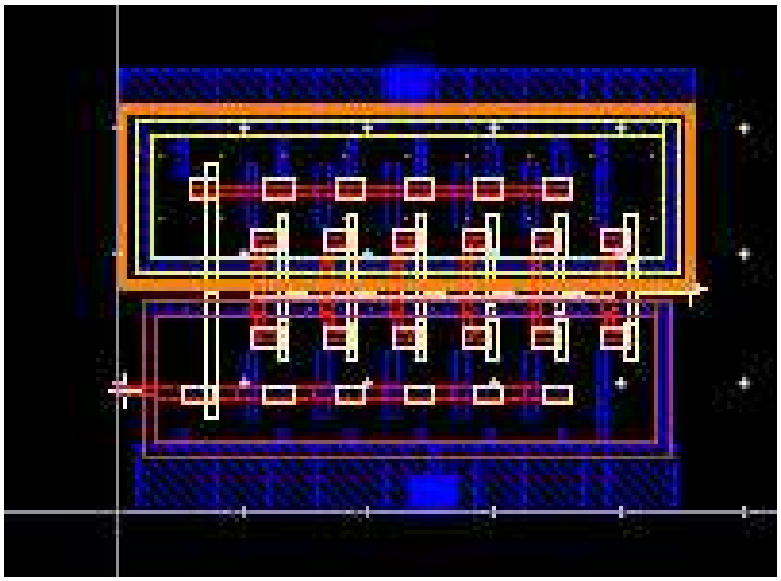

Fig.17: Extracted view of VCO

Table 2. Performance Summary and comparison

Parameter	Specification			
	Ref[15]	Ref[16]	Ref[17]	This Work
Technology (CMOS)	180 nm	180 nm	180 nm	180 nm
Operating voltage (V)	1.8	1.8	1.8	0.6
Gain (K_{VCO}) (GHz/V)	-	-	-	0.453
Tuning range	0.818 GHz - 1.325 GHz	22.74 GHz – 24.63 GHz	53 MHz – 2.348 GHz	9.371 MHz – 94.73 MHz
Inverter delay (ps)	-	-	35	190.4
Power dissipation (µW)	467	2400	848	0.939
Phase noise (dBc/Hz)	-	-102.4	-	-92.25
No. of stages	5	1	3	5
Die area	-	-	-	393.72 μm^2

V. Conclusion and Future Work

The design has been presented in a 180nm CMOS technology and is designed using CMOS inverter with current mirror. The VCO dissipates power around 939.5546 nW for 0.6 V supply with a phase noise of -92.25 dBc/Hz and tuning range of 79.95%. The overall area consumed is about 393.72 μm^2. This work can be extended further by optimizing the design to achieve improved performance for different applications as well as by implementing the same at system level.

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